

S/N 10/004,661PATENTIN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Thomas A. Figura

Examiner: Yennhu Huynh

Serial No.: 10/004,661

Group Art Unit: 2813

Filed: December 4, 2001

Docket: 303.645US3

Title: METHOD AND STRUCTURE FOR IMPROVED ALIGNMENT TOLERANCE  
IN MULTIPLE, SINGULARIZED PLUGS**FAX RECEIVED**SUPPLEMENTAL AMENDMENT

MAR 20 2003

TECHNOLOGY CENTER 2800

Commissioner for Patents  
Washington, D.C. 20231

Based on a discussion with the Examiner on March 19, 2003 regarding the allowability of the claims, please amend the above-identified patent application as follows.

IN THE CLAIMS

1. (Currently Amended) An integrated circuit device on a substrate, comprising:  
multiple semiconductor surface structures spaced apart along the substrate;  
a number of plugs contacting the substrate between the multiple semiconductor surface structures, wherein the number of plugs includes an inner plug and a pair of outer plugs  
a pair of spacers placed on interior walls of an opening at the inner plug, the pair of spacers separating the inner plug and the pair of outer plugs, the inner plug being isolated  
(beneath and between an adjacent pair of the semiconductor surface structures, the pair of outer  
plugs covering part of top portions of the adjacent pair; and  
a conductive material contacted the inner plug and being isolated from the pair of outer  
plugs by the pair of spacers, wherein the inner and the pair of outer plugs are formed by the  
method of:

forming a ~~first~~ an initial opening in a first isolation layer on the multiple semiconductor surface structures, wherein forming the ~~first~~ initial opening includes exposing portions of the multiple semiconductor surface structures, and includes exposing portions of the substrate between the multiple semiconductor surface structures;

depositing a ~~first~~ an initial conductive material in the ~~first~~ initial opening to cover the multiple semiconductor surface structures;

forming a second isolation layer across the ~~first~~ initial conductive material; and

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Hueish  
3/24/03

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March 20, 2003

MAR 20 2003

Time: 11:15AM  
(Minneapolis, Minn.)

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TO: Commissioner for Patents  
Attn: Yennhu Huynh  
Patent Examining Corps  
Facsimile Center  
Washington, D.C. 20231

FROM: Viet Tong

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Attached please find the supplemental amendment to the claims.

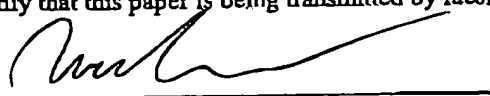
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By: 

Name: Viet V. Tong

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I hereby certify that this paper is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date shown below.

  
Viet V. Tong

3-20-03  
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